In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) A reading method for a memory device comprising an array memory cell and a reference memory cell comprising:

biasing said array memory cell and said reference memory cell so as to modify their respective current-conduction states in different instants; and

determining ~~the~~ contents of said array memory cell on ~~the~~ a basis of the temporal relation existing between the instants when the current-conduction states of said array memory cell and of said reference memory cell are modified.

2. (Currently Amended) The reading method according to claim 1, wherein said temporal relation is defined by ~~the~~ a modification order of the current-conduction states of said array memory cell and said reference memory cell.

3. (Previously Presented) The reading method according to claim 1, wherein said step of biasing said array memory cell and said reference memory cell comprises the step of:

applying a same reading voltage having a time-variable pattern to control terminals of said array memory cell and said reference memory cell.

4. (Previously Presented) The reading method according to claim 3, wherein said reading voltage has a substantially ramp-like time pattern.

5. (Previously Presented) The reading method according to claim 4, wherein said substantially ramp-like time pattern is increasing in time.

6. (Currently Amended) The reading method according to claim 1, wherein said step of determining the contents of said array memory cell comprises the step of:

comparing ~~the~~ a cell current of said array memory cell and ~~the~~ a reference current of said reference memory cell with a same comparison current, thereby generating a cell-latch signal

and, respectively, a reference-latch signal containing information on the instants when said cell current and, respectively, said reference current satisfy a preset relation with said comparison current; and

determining the contents of said array memory cell on the basis of the temporal relation between the instants when said cell current and said reference current satisfy said preset relation.

7. (Currently Amended) The reading method according to claim 6, wherein said preset relation is defined by ~~the~~ a condition that said cell current or said reference current exceeds said comparison current.

8. (Previously Presented) The reading method according to claim 6, wherein said cell-latch signal and said reference-latch signal are logic type signals switching from a first to a second logic level when said cell current and, respectively, said reference current satisfy said preset relation.

9. (Previously Presented) The reading method according to claim 6, further comprising turning off said array memory cell and said reference memory cell immediately after said preset relation has been satisfied.

10. (Currently Amended) A memory device comprising an array memory cell and a reference memory cell, comprising:

biasing means for biasing said array memory cell and said reference memory cell so as to modify their respective current-conduction states in different instants of time; and

evaluation means for determining ~~the~~ contents of said array memory cell on ~~the~~ a basis of the temporal relation existing between the instants when the current-conduction states of said array memory cell and of said reference memory cell are modified.

11. (Previously Presented) The memory device according to claim 10, wherein said temporal relation is defined by the modification order of the current-conduction states of said array memory cell and of said reference memory cell.

12. (Previously Presented) The memory device according to claim 10, wherein said biasing means comprises:

voltage-generating means for supplying control terminals of said array memory cell and of said reference memory cell with a same reading voltage having a time-variable pattern.

13. (Previously Presented) The memory device according to claim 12, wherein said reading voltage presents a substantially ramp-like time pattern.

14. (Previously Presented) The memory device according to claim 13, wherein said substantially ramp-like time pattern is increasing in time.

15. (Currently Amended) The memory device according to claim 10, wherein said evaluation means comprises:

comparator means for comparing ~~the~~ a cell current of said array memory cell and ~~the~~ a reference current of said reference memory cell with a same comparison current, thereby generating a cell-latch signal and, respectively, a reference-latch signal containing information on the instants when said cell current and, respectively, said reference current satisfy a preset relation with said comparison current; and

determination means for determining the contents of said array memory cell on the basis of the temporal relation between the instants when said cell current and said reference current satisfy said preset relation.

16. (Previously Presented) The memory device according to claim 15, wherein said preset relation is defined by the condition that said cell current or said reference current exceed said comparison current.

17. (Previously Presented) The memory device according to claim 15, wherein said cell-latch signal and said reference-latch signal are logic type signals switching from a first to a second logic level when said cell current and, respectively, said reference current satisfy said preset relation.

18. (Previously Presented) The memory device according to claim 15, further comprising turning-off means for turning off said array memory cell and said reference memory cell immediately after said preset relation has been satisfied.

19. (Previously Presented) The memory device according to claim 15, further comprising bus means for carrying said cell-latch and reference-latch signals.